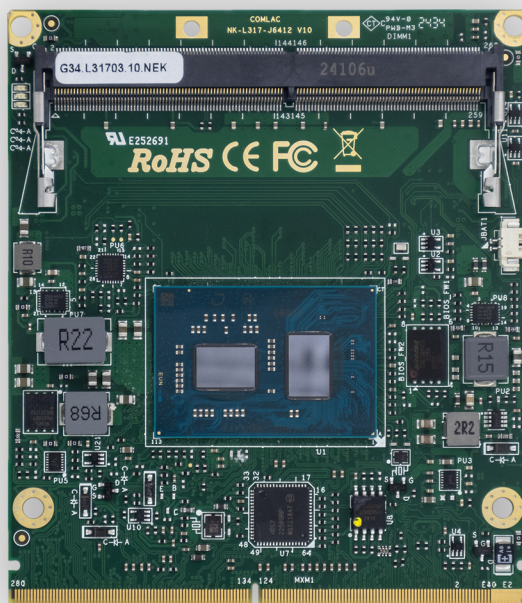




# NK-L317-J6412

## User Manual

 Small size, modular design

 MXM3.0 high-speed connector

 NODKA custom signal specification

 High reliability installation method

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    - Product name and serial number
    - Description of peripheral devices
    - Description of user software (operating system, version, application software, etc.)
    - Complete description of the problem encountered
    - Complete content of any error messages
-

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## Safety Instructions

- Please read these safety instructions carefully.
  - Please keep this user manual for future reference.
  - Before cleaning the device with a damp cloth, unplug the power cord from the socket. Do not use liquid or spray cleaners to clean the device.
  - The power socket should be installed near the device for easy connection; avoid stepping on the power cord, especially at the plug, socket, or connection points on the device.
  - Do not use the device in a humid environment.
  - Do not place the device near heat sources such as radiators, heat registers, stoves, or other heat-producing devices (including amplifiers).
  - Before installation, ensure the device is placed on a stable surface. Accidental drops may cause damage to the device.
  - The openings on the device casing are for air convection to prevent overheating. Do not cover these openings.
  - When connecting the device to a power adapter, please follow the rated input voltage and current markings on the device. Do not use a power adapter that is not provided with the product or does not match the specifications. Due to differences in circuit design, using an incompatible power adapter may damage internal components.
  - Before connecting the device to a power socket, ensure the voltage of the power socket meets the requirements. Read, note, and follow all safety instructions to ensure proper and safe installation and connection of the device.
  - Place the power cord in a location where it is not easily tripped over, and do not cover the power cord with any objects.
  - Please pay attention to all warning labels on the device.
  - If the device is not used for a long time, disconnect it from the power socket to avoid damage from excessive voltage fluctuations.
  - Do not allow any liquid to enter the ventilation openings to prevent fire or short circuits.
  - Do not open the device by yourself; for your safety, please have the device opened by a certified engineer.
  - If any of the following situations occur, please have the device repaired by a professional:
    - The power cord or plug is damaged
    - Liquid has entered the device
    - The device has been exposed to a highly humid environment
    - The device is not functioning properly, or you cannot get it to work properly using the user manual
    - The device has been dropped or damaged
    - The device has obvious external damage
  - If the product is a display screen, do not apply excessive pressure to the screen, as this may cause permanent damage to the screen.
  - Do not place the device in an environment outside the recommended storage temperature range, i.e., below -40° C (40° F) or above 85° C (185° F), as this may damage the device.
  - Any unverified components may cause unexpected damage to the device. To ensure proper installation, only use the components provided in the accessory box, such as screws.
  - Note: The computer is equipped with a battery-powered real-time clock circuit. If the battery is replaced incorrectly, there is a risk of explosion. Therefore, only use the same type or equivalent battery recommended by the manufacturer for replacement. Please follow the manufacturer's instructions for disposing of old batteries.
  - Whenever performing hardware operations, be sure to completely disconnect the chassis power. When the device is powered on, do not change any connections or configurations to avoid damaging sensitive electronic components due to sudden power surges.
  - Avoid direct sunlight on the display screen and keep it away from strong light and other heat sources. Prolonged exposure to such environments may cause the display screen to fade and be damaged.
  - If consumers use a power adapter for charging, they should purchase a power adapter that is certified by CCC and meets standard requirements.
  - Warning: Operating this device in a residential environment may cause radio interference.
-

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## Warnings and Notes



- Warning to users: There are non-insulated dangerous voltages inside the product, which may cause electric shock.
- During operation, users must pay special attention to the warning information in this manual to avoid personal injury.
- Maintenance information is for authorized service personnel only. To reduce the risk of electric shock, do not perform any maintenance other than the provided operating information unless authorized.
- To reduce the risk of electric shock, do not disassemble the casing (or back). There are no user-serviceable parts inside the device. Please consult authorized service personnel for service information.

The notes in this manual help users avoid hardware damage or data loss. For example, if the battery is replaced incorrectly, there is a risk of explosion. Therefore, only use the same type or equivalent battery recommended by the manufacturer for replacement. Please follow the manufacturer's instructions for disposing of old batteries.



### Maintenance Warnings

Warning: Maintenance information is for authorized service personnel only. To reduce the risk of electric shock, do not perform any maintenance other than the provided operating information unless authorized.

Warning: To reduce the risk of electric shock, do not disassemble the casing (or back). There are no user-serviceable parts inside the device. Please consult authorized service personnel for service information.

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## Chapter 1 Product Introduction

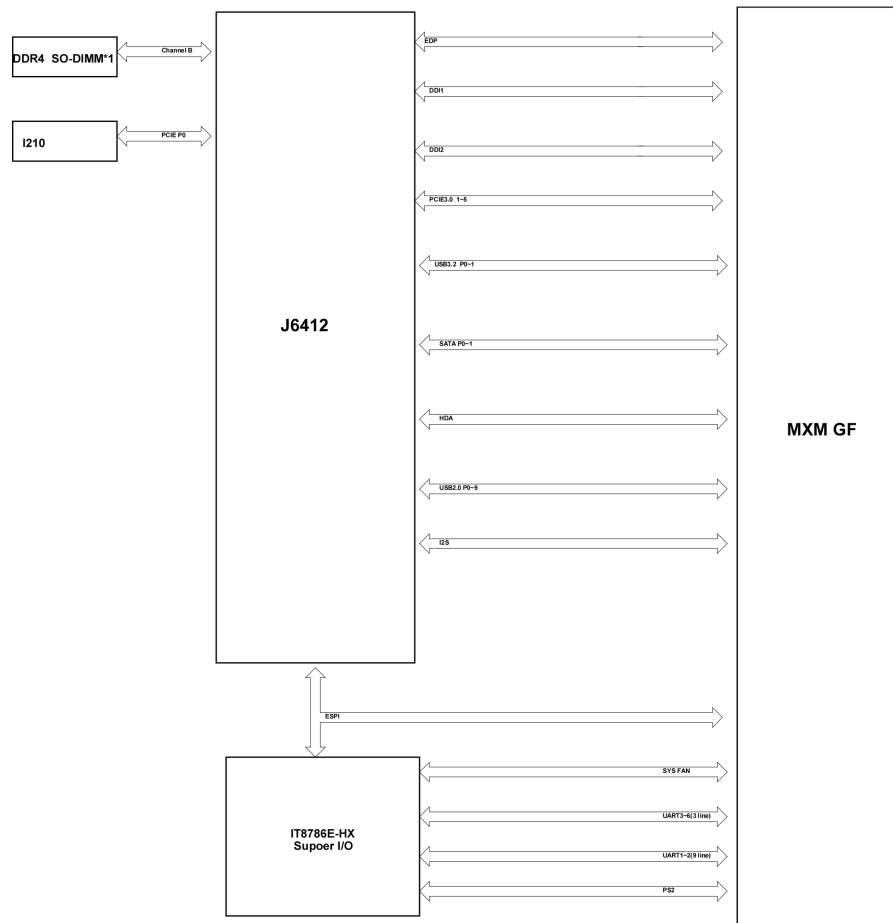
### 1.1 Product Brief Description

NK-L317-J6412 base Intel® Celeron® J6412 processor, Quad-core, base frequency 2.0GHz up to 2.6GHz , TDP 10W ,Support 1 x DDR4-3200MHz SO-DIMM slot, up to 32GB,Support 2 x DDI,1 x eDP, Tri-Display,Type3 Interface Signals with MXM3.0 Gold Finger .

### 1.2 Product Specifications

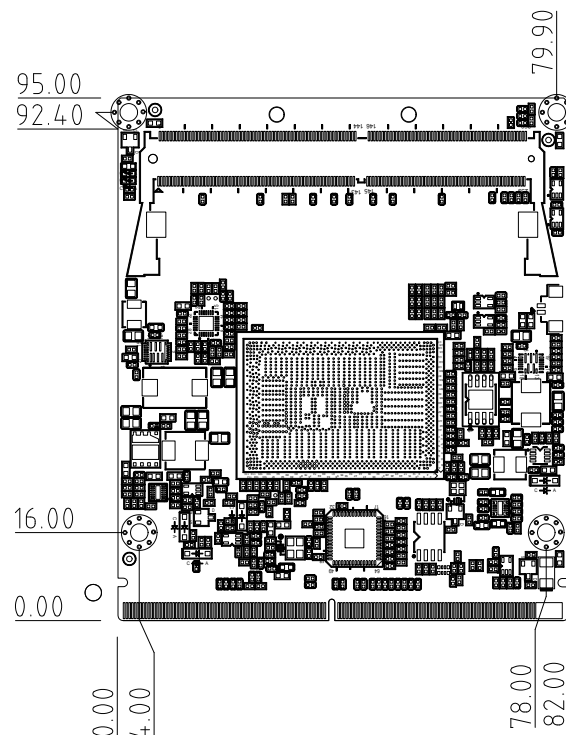
| Project           |                 | Content                                                                                  |
|-------------------|-----------------|------------------------------------------------------------------------------------------|
| Processor System  | CPU             | Intel® Celeron® J6412 processor, Quad-core, base frequency 2.0GHz up to 2.6GHz , TDP 10W |
|                   | Chipset         | Intel® SoC integrated                                                                    |
|                   | BIOS            | AMI 256Mb UEFI BIOS                                                                      |
| Memory            | Technology      | Single Channel(Non-ECC) DDR4-3200MHz, up to 32GB                                         |
|                   | Slot            | 1 x DDR4 SO-DIMM slot                                                                    |
| Graphic           | Controller      | Intel HD graphics integrated                                                             |
| Expansion Signals | Display         | 2 x DDI,1 x eDP                                                                          |
|                   | Serial Port     | 2 x Uart(9 line),4 x Uart(3 line)                                                        |
|                   | USB             | 2 x USB3.0 ,8x USB2.0                                                                    |
|                   | SATA            | 2 x SATA 3.0                                                                             |
|                   | PCIe            | 5 port 5lanes (1 X2、 3 X1)                                                               |
|                   | GPIO            | 1 x 4bit GPIO                                                                            |
|                   | Audio           | 1 x Intel HDA Audio codec                                                                |
|                   | Smart Fan       | 1 x Smart Fan                                                                            |
|                   | Ethernet        | Intel i210AT Controller                                                                  |
|                   | others          | 1 x eSPI,1 x I <sup>2</sup> C,1 x SMBus,1 x Buzzer, 1 x KB/MS                            |
| Watchdog Timer    | Output&Interval | System reset, programmable from 1~255 seconds                                            |
| Power             | Power input     | 5V                                                                                       |
| OS Support        | MS Windows      | Windows 10/11                                                                            |
|                   | Linux           | Linux                                                                                    |
| Mechanism         | 尺寸 Dimensions   | (L)95mm x (W)82mm                                                                        |
|                   | Gross Weight    | 0.04kg                                                                                   |
| Environment       | Temperature     | Operating: 0°C ~60°C with SSD                                                            |
|                   |                 | Storage: -40°C ~85°C                                                                     |
|                   | Humidity        | 5~95% (Non-condensing)                                                                   |
|                   | Vibration       | 5~500Hz, 3Grms operating                                                                 |

### 1.3 Block Diagram



### 1.4 Mechanical Drawing

#### 1.4.1 Motherboard Front Dimensional Drawing



1.5 Packaging List

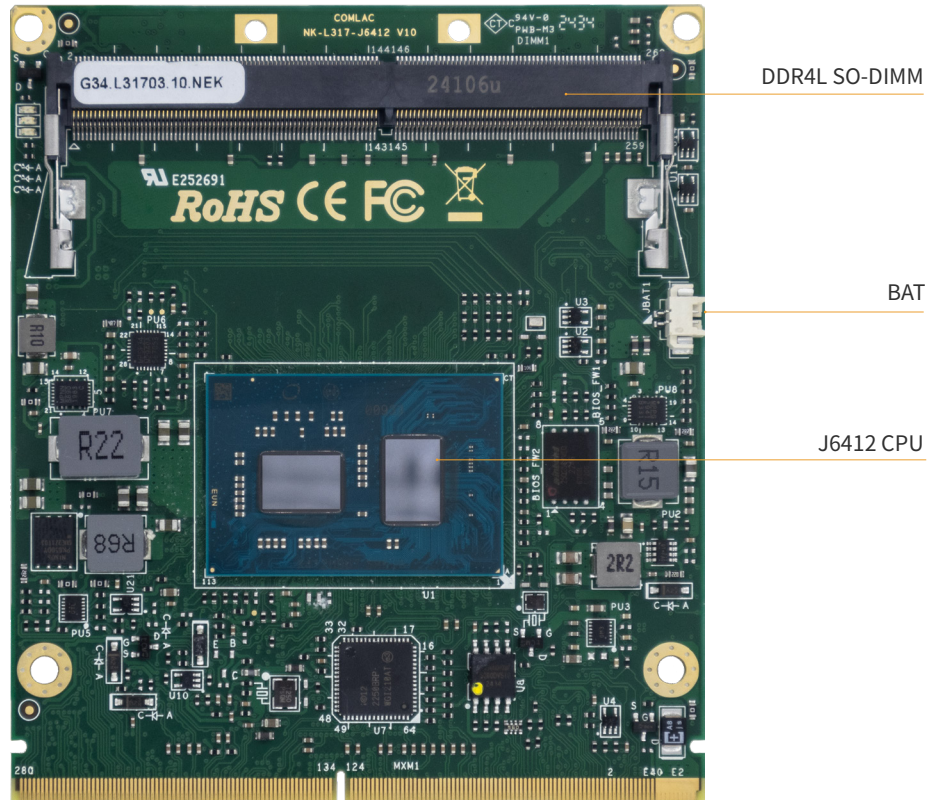
1.5.1 Ordering Information

| Part No.          | Model         | Description                                         |
|-------------------|---------------|-----------------------------------------------------|
| F34.L31703.00.NEK | NK-L317-J6412 | Type3, 95*82mm Elkhart Lake, J6412, 1x DDR4 SO-DIMM |

## Chapter 2 Interface Introduction

### 2.1 Interface Introduction

The interfaces on the motherboard are only internal interfaces. The internal interfaces need to be connected to the equipment through wires to realize the corresponding functions. The interface positions are as shown in the figure below:



### 2.2 Battery

A default RTC Battery is provided to power the RTC system. If not in use, the carrier board needs to provide an RTC Battery for power supply, which is connected to VBAT\_J. The pin definition is as follows:

| Battery Pin Definition |           |     |          |
|------------------------|-----------|-----|----------|
| Pin                    | Pin Name  | Pin | Pin Name |
| 1                      | VBAT_J /+ | 2   | GND/-    |

### 2.3 DDR4-SO DIMM

The DDR4 SO-DIMM interface has a total of 260 pins. The pins include power, address control, data, reference calibration, etc., which are responsible for power supply, transmission of command data, and calibration signals to ensure the efficient and stable operation of the memory. It can achieve high-bandwidth and low-power data storage and transmission to meet the memory performance requirements of mobile devices.

## 2.4 MXM3.0 Pin Definition

| MXM NO. | Type | Function         | Remark                                                                        |
|---------|------|------------------|-------------------------------------------------------------------------------|
| E1      | S    | 5V Standby Power | Stable 5V Power Supply                                                        |
| E2      | S    | 5V Standby Power | Stable 5V Power Supply                                                        |
| E3      | S    | GND              | Power Ground                                                                  |
| 1       | I    | BOARD_PWROK      | Carrier Board Power S0 Indicator Signal(Pulled low if there is a problem)     |
| 3       | O    | MXM_HDA_SYNC     | HDA Audio Signal (to Audio Codec Extension HP/MIC)                            |
| 5       | O    | MXM_HDA_BIT_CLK  | HDA Audio Signal (to Audio Codec Extension HP/MIC)                            |
| 7       | O    | MXM_HDA_SDOUT    | HDA Audio Signal (to Audio Codec Extension HP/MIC)                            |
| 9       | I    | MXM_HDA_SDIN     | HDA Audio Signal (to Audio Codec Extension HP/MIC)                            |
| 11      | O    | MXM_HDA_RST#     | HDA Audio Signal (to Audio Codec Extension HP/MIC)                            |
| 13      | S    | GND              | Signal Ground                                                                 |
| 15      | S    | PVCC_SDIO        | SD Card Power Supply(Provided by Core Board to Carrier Board SD Card)         |
| 17      | IO   | MXM_SD_CMD       | SD Card Command Line(For command transmission between host and SD card)       |
| 19      | IO   | MXM_SD_D0        | Data Line 0(For data transmission)                                            |
| 21      | IO   | MXM_SD_D1        | Data Line 1(For data transmission)                                            |
| 23      | IO   | MXM_SD_D2        | Data Line 2(For data transmission)                                            |
| 25      | IO   | MXM_SD_D3        | Data Line 3(For data transmission)                                            |
| 27      | IO   | MXM_SD_D0        | Data Line 0(For data transmission)                                            |
| 29      | I    | MXM_SD_CD        | SD Card Insertion Detection                                                   |
| 31      | O    | MXM_SD_CLK       | SD Card Clock Signal(Synchronizes data transmission between host and SD card) |
| 33      | I    | MXM_SD_WP        | SD Card Write Protect Indicator                                               |
| 35      | I    | MXM_SD_PWR_EN    | SDIO Interface Power Switch Control                                           |
| 37      | S    | GND              | Signal Ground                                                                 |
| 39      | IO   | SIO_GPIO70       | Programmable GPIO                                                             |
| 41      | IO   | SIO_GPIO71       | Programmable GPIO                                                             |
| 43      | IO   | SIO_GPIO72       | Programmable GPIO                                                             |
| 45      | IO   | SIO_GPIO73       | Programmable GPIO                                                             |
| 47      | I    | MXM_FANTAC2      | Fan Speed Detection Signal                                                    |
| 49      | O    | MXM_FANPWM2      | Fan Speed Control Signal                                                      |
| 51      | S    | GND              | Signal Ground                                                                 |
| 53      | IO   | USB_N2           | Core Board USB2.0 lane 2 Data Negative Signal (USB2_CH2_DN)                   |
| 55      | IO   | USB_P2           | Core Board USB2.0 lane 2 Data Positive Signal (USB2_CH2_DP)                   |
| 57      | IO   | USB_N4           | Core Board USB2.0 lane 4 Data Negative Signal (USB2_CH4_DN)                   |
| 59      | IO   | USB_P4           | Core Board USB2.0 lane 4 Data Positive Signal (USB2_CH4_DP)                   |
| 61      | S    | GND              | Signal Ground                                                                 |
| 63      | IO   | USB_P1           | Core Board USB2.0 lane 1 Data Negative Signal (USB2_CH1_DN)                   |
| 65      | IO   | USB_N1           | Core Board USB2.0 lane 1 Data Positive Signal (USB2_CH1_DP)                   |
| 67      | IO   | USB_N0           | Core Board USB2.0 lane 0 Data Negative Signal (USB2_CH0_DN)                   |
| 69      | IO   | USB_P0           | Core Board USB2.0 lane 0 Data Positive Signal (USB2_CH0_DP)                   |

| MXM NO. | Type | Function      | Remark                                                                                             |
|---------|------|---------------|----------------------------------------------------------------------------------------------------|
| 71      | S    | GND           | Signal Ground                                                                                      |
| 73      | I    | USB3_RX1_N    | Core Board USB3.0 lane 1 Receive Negative Signal (USB3_CH1_RXN)                                    |
| 75      | I    | USB3_RX1_P    | Core Board USB3.0 lane 1 Receive Positive Signal (USB3_CH1_RXP)                                    |
| 77      | S    | GND           | Signal Ground                                                                                      |
| 79      | I    | USB3_RX0_N    | Core Board USB3.0 lane 0 Receive Negative Signal (USB3_CH0_RXN)                                    |
| 81      | I    | USB3_RX0_P    | Core Board USB3.0 lane 0 Receive Positive Signal (USB3_CH0_RXP)                                    |
| 83      | S    | GND           | Signal Ground                                                                                      |
| 85      | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| 87      | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| 89      | S    | GND           | Signal Ground                                                                                      |
| E40     | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| E41     | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| E42     | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| E43     | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| E44     | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| E45     | /    | NC            | Reserved Pin (Leave floating)                                                                      |
| E46     | O    | PMC_SLP_S3_N  | CPU Sleep Signal(Low during sleep, High during normal operation)                                   |
| E47     | O    | PMC_SLP_S4_N  | CPU Hibernate Signal(Low during hibernation, High during normal operation)                         |
| E48     | I    | RTC_TEST_N    | RTC Reset Signal(Connect to low for Clear CMOS, leave floating during normal use)                  |
| E49     | I    | VBAT_J        | RTC Battery Power                                                                                  |
| 2       | I    | MXM_PWR_ON    | Power Button Signal(Connect to switch on carrier board, low pulse $\geq 100\text{ms}$ to power on) |
| 4       | I    | MXM_RESET     | System Reset Signal(For system reboot, low pulse $\geq 100\text{ms}$ to take effect)               |
| 6       | O    | MXM_PS_ON#    | Carrier Board S0 Power Enable Control(Active low)                                                  |
| 8       | O    | PCIRST_MXM    | Reset All Devices(Active high)                                                                     |
| 10      | I    | PMC_WAKE_N    | Wake-up Signal(Low pulse from carrier board to wake system)                                        |
| 12      | O    | SATA_LED_N    | SATA Activity LED Indicator(Active low)                                                            |
| 14      | O    | SPKR          | Buzzer Signal(For motherboard status indication, connect to buzzer on carrier board)               |
| 16      | O    | SIO_PME#      | SIO PME Signal Output(Active low pulse, leave floating if unused)                                  |
| 18      | S    | GND           | Ground                                                                                             |
| 20      | IO   | MXM_SMB_DATA  | SMBUS Data Bus                                                                                     |
| 22      | O    | MXM_SMB_CLK   | SMBUS Clock Bus                                                                                    |
| 24      | O    | MXM_I2C0_SCL  | I2C Clock Signal                                                                                   |
| 26      | IO   | MXM_I2C0_SDA  | I2C Data Signal                                                                                    |
| 28      | O    | MXM_ESPI_CLK  | Clock Signal                                                                                       |
| 30      | IO   | MXM_ESPI_AD3  | ESPI Address/Data Line 3                                                                           |
| 32      | IO   | MXM_ESPI_AD2  | ESPI Address/Data Line 2                                                                           |
| 34      | IO   | MXM_ESPI_AD1  | ESPI Address/Data Line 1                                                                           |
| 36      | IO   | MXM_ESPI_AD0  | ESPI Address/Data Line 0                                                                           |
| 38      | I    | ESPI_CS1_N    | ESPI Chip Select 1 (CS1#, Active Low)                                                              |
| 40      | I    | ESPI_ALERT1_N | ESPI Alert Signal (Active Low)                                                                     |
| 42      | IO   | MXM_MS DAT    | PS/2 Mouse Data Signal                                                                             |

| MXM NO. | Type | Function   | Remark                                                           |
|---------|------|------------|------------------------------------------------------------------|
| 44      | IO   | MXM_MSCLK  | PS/2 Mouse Clock Signal                                          |
| 46      | IO   | MXM_KBKDAT | PS/2 Keyboard Data Signal                                        |
| 48      | IO   | MXM_KBCLK  | PS/2 Keyboard Clock Signal                                       |
| 50      | S    | GND        | Signal Ground                                                    |
| 52      | IO   | USB_N6     | Core Board USB2.0 lane 6 Data Negative Signal (USB2_CH6_DN)      |
| 54      | IO   | USB_P6     | Core Board USB2.0 lane 6 Data Positive Signal (USB2_CH6_DP)      |
| 56      | IO   | USB_N7     | Core Board USB2.0 lane 7 Data Negative Signal (USB2_CH7_DN)      |
| 58      | IO   | USB_P7     | Core Board USB2.0 lane 7 Data Positive Signal (USB2_CH7_DP)      |
| 60      | S    | GND        | Signal Ground                                                    |
| 62      | IO   | USB_N5     | Core Board USB2.0 lane 5 Data Negative Signal (USB2_CH5_DN)      |
| 64      | IO   | USB_P5     | Core Board USB2.0 lane 5 Data Positive Signal (USB2_CH5_DP)      |
| 66      | IO   | USB_N3     | Core Board USB2.0 lane 3 Data Negative Signal (USB2_CH3_DN)      |
| 68      | IO   | USB_P3     | Core Board USB2.0 lane 3 Data Positive Signal (USB2_CH3_DP)      |
| 70      | S    | GND        | Signal Ground                                                    |
| 72      | O    | USB3_TX0_N | Core Board USB3.0 lane 0 Transmit Negative Signal (USB3_CH0_TXN) |
| 74      | O    | USB3_TX0_P | Core Board USB3.0 lane 0 Transmit Positive Signal (USB3_CH0_TXP) |
| 76      | S    | GND        | Signal Ground                                                    |
| 78      | O    | USB3_TX1_N | Core Board USB3.0 lane 1 Transmit Negative Signal (USB3_CH1_TXN) |
| 80      | O    | USB3_TX1_P | Core Board USB3.0 lane 1 Transmit Positive Signal (USB3_CH1_TXP) |
| 82      | S    | GND        | Signal Ground                                                    |
| 84      | /    | NC         | Reserved Pin (Leave floating)                                    |
| 86      | /    | NC         | Reserved Pin (Leave floating)                                    |
| 88      | S    | GND        | Signal Ground                                                    |
| 90      | /    | NC         | Reserved Pin (Leave floating)                                    |
| 91      | /    | NC         | Reserved Pin (Leave floating)                                    |
| 93      | /    | NC         | Reserved Pin (Leave floating)                                    |
| 95      | S    | GND        | Signal Ground                                                    |
| 97      | I    | PCIE1_RXN  | Core Board PCIe Lane 1 Receive Negative Signal (PCIe_RX1_N)      |
| 99      | I    | PCIE1_RXP  | Core Board PCIe Lane 1 Receive Positive Signal (PCIe_RX1_P)      |
| 101     | I    | PCIE2_RXN  | Core Board PCIe Lane 2 Receive Negative Signal (PCIe_RX2_N)      |
| 103     | I    | PCIE2_RXP  | Core Board PCIe Lane 2 Receive Positive Signal (PCIe_RX2_P)      |
| 105     | S    | GND        | Signal Ground                                                    |
| 107     | I    | PCIE3_RXN  | Core Board PCIe Lane 3 Receive Negative Signal (PCIe_RX3_N)      |
| 109     | I    | PCIE3_RXP  | Core Board PCIe Lane 3 Receive Positive Signal (PCIe_RX3_P)      |
| 111     | S    | GND        | Signal Ground                                                    |
| 113     | O    | CLK0_DN    | Core Board PCIe lane Clock Negative Signal (PCIe_CLK_N)          |
| 115     | O    | CLK0_DP    | Core Board PCIe lane Clock Positive Signal (PCIe_CLK_P)          |
| 117     | O    | CLK1_DN    | Core Board PCIe lane Clock Negative Signal (PCIe_CLK_N)          |
| 119     | O    | CLK1_DP    | Core Board PCIe lane Clock Positive Signal (PCIe_CLK_P)          |
| 121     | S    | GND        | Signal Ground                                                    |
| 123     | I    | PCIE5_RXN  | Core Board PCIe Lane 5 Receive Negative Signal (PCIe_RX5_N)      |

| MXM NO. | Type | Function      | Remark                                                       |
|---------|------|---------------|--------------------------------------------------------------|
| 125     | I    | PCIE5_RXP     | Core Board PCIe Lane 5 Receive Positive Signal (PCle_RX5_P)  |
| 133     | S    | GND           | Signal Ground                                                |
| 135     | I    | ESPI_RST_N    | ESPI Reset Signal (Active Low)                               |
| 137     | I    | MXM_I2S_RXD   | Serial Data Input (SDATA_IN) for connecting to I2S devices   |
| 139     | O    | MXM_I2S_SCLK  | Bit Clock (BCLK/SCK) for connecting to I2S devices           |
| 141     | O    | MXM_I2S_TXD   | Serial Data Output (SDATA_OUT) for connecting to I2S devices |
| 143     | O    | MXM_I2S_SFRM  | Frame Clock (LRCK/FS) for connecting to I2S devices          |
| 145     | O    | MXM_I2S_MCLK1 | I2S Master Clock (MCLK)                                      |
| 147     | I    | ESPI_CS0_N    | ESPI Chip Select 0 (CS0#, Active Low)                        |
| 149     | S    | GND           | Signal Ground                                                |
| 151     | I    | PCIE4_RXN     | Core Board PCIe Lane 4 Receive Negative Signal (PCle_RX4_N)  |
| 153     | I    | PCIE4_RXP     | Core Board PCIe Lane 4 Receive Positive Signal (PCle_RX4_P)  |
| 155     | /    | NC            | Reserved Pin (Leave floating)                                |
| 157     | /    | NC            | Reserved Pin (Leave floating)                                |
| 159     | S    | GND           | Signal Ground                                                |
| 161     | /    | NC            | Reserved Pin (Leave floating)                                |
| 163     | /    | NC            | Reserved Pin (Leave floating)                                |
| 165     | /    | NC            | Reserved Pin (Leave floating)                                |
| 167     | /    | NC            | Reserved Pin (Leave floating)                                |
| 169     | S    | GND           | Signal Ground                                                |
| 171     | IO   | LAN1_MDI_P3   | Network MDI lane 3 Positive Signal (MDI3_P)                  |
| 173     | IO   | LAN1_MDI_N3   | Network MDI lane 3 Negative Signal (MDI3_N)                  |
| 175     | IO   | LAN1_MDI_P2   | Network MDI lane 2 Positive Signal (MDI2_P)                  |
| 177     | IO   | LAN1_MDI_N2   | Network MDI lane 2 Negative Signal (MDI2_N)                  |
| 179     | S    | GND           | Signal Ground                                                |
| 181     | IO   | LAN1_MDI_P1   | Network MDI lane 1 Positive Signal (MDI1_P)                  |
| 183     | IO   | LAN1_MDI_N1   | Network MDI lane 1 Negative Signal (MDI1_N)                  |
| 185     | IO   | LAN1_MDI_P0   | Network MDI lane 0 Positive Signal (MDI0_P)                  |
| 187     | IO   | LAN1_MDI_N0   | Network MDI lane 0 Negative Signal (MDI0_N)                  |
| 92      | /    | NC            | Reserved Pin (Leave floating)                                |
| 94      | S    | GND           | Signal Ground                                                |
| 96      | O    | PCIE1_TXN     | Core Board PCIe Lane 1 Transmit Negative Signal (PCle_TX1_N) |
| 98      | O    | PCIE1_TXP     | Core Board PCIe Lane 1 Transmit Positive Signal (PCle_TX1_P) |
| 100     | O    | PCIE2_TXP     | Core Board PCIe Lane 2 Transmit Positive Signal (PCle_TX2_P) |
| 102     | O    | PCIE2_TXN     | Core Board PCIe Lane 2 Transmit Negative Signal (PCle_TX2_N) |
| 104     | S    | GND           | Signal Ground                                                |
| 106     | O    | PCIE3_TXP     | Core Board PCIe Lane 3 Transmit Positive Signal (PCle_TX3_P) |
| 108     | O    | PCIE3_TXN     | Core Board PCIe Lane 3 Transmit Negative Signal (PCle_TX3_N) |
| 110     | S    | GND           | Signal Ground                                                |
| 112     | O    | CLK2_DN       | Core Board PCIe lane Clock Negative Signal (PCle_CLK_N)      |
| 114     | O    | CLK2_DP       | Core Board PCIe lane Clock Positive Signal (PCle_CLK_P)      |
| 116     | O    | CLK3_DN       | Core Board PCIe lane Clock Negative Signal (PCle_CLK_N)      |

| MXM NO. | Type | Function      | Remark                                                       |
|---------|------|---------------|--------------------------------------------------------------|
| 118     | O    | CLK3_DP       | Core Board PCIe lane Clock Positive Signal (PCIe_CLK_P)      |
| 120     | S    | GND           | Signal Ground                                                |
| 122     | O    | PCIE5_TXN     | Core Board PCIe Lane 5 Transmit Negative Signal (PCIe_TX5_N) |
| 124     | O    | PCIE5_TXP     | Core Board PCIe Lane 5 Transmit Positive Signal (PCIe_TX5_P) |
| 134     | S    | GND           | Signal Ground                                                |
| 136     | IO   | USB_N8        | Core Board USB2.0 lane 8 Data Negative Signal (USB2_CH8_DN)  |
| 138     | IO   | USB_P8        | Core Board USB2.0 lane 8 Data Positive Signal (USB2_CH8_DP)  |
| 140     | IO   | USB_N9        | Core Board USB2.0 lane 9 Data Negative Signal (USB2_CH9_DN)  |
| 142     | IO   | USB_P9        | Core Board USB2.0 lane 9 Data Positive Signal (USB2_CH9_DP)  |
| 144     | /    | NC            | Reserved Pin (Leave floating)                                |
| 146     | /    | NC            | Reserved Pin (Leave floating)                                |
| 148     | /    | NC            | Reserved Pin (Leave floating)                                |
| 150     | S    | GND           | Signal Ground                                                |
| 152     | O    | PCIE4_TXP     | Core Board PCIe Lane 4 Transmit Positive Signal (PCIe_TX4_P) |
| 154     | O    | PCIE4_TXN     | Core Board PCIe Lane 4 Transmit Negative Signal (PCIe_TX4_N) |
| 156     | /    | NC            | Reserved Pin (Leave floating)                                |
| 158     | /    | NC            | Reserved Pin (Leave floating)                                |
| 160     | S    | GND           | Signal Ground                                                |
| 162     | /    | NC            | Reserved Pin (Leave floating)                                |
| 164     | /    | NC            | Reserved Pin (Leave floating)                                |
| 166     | /    | NC            | Reserved Pin (Leave floating)                                |
| 168     | /    | NC            | Reserved Pin (Leave floating)                                |
| 170     | S    | GND           | Signal Ground                                                |
| 172     | O    | CLK4_DN       | Core Board PCIe lane Clock Negative Signal (PCIe_CLK_N)      |
| 174     | O    | CLK4_DP       | Core Board PCIe lane Clock Positive Signal (PCIe_CLK_P)      |
| 176     | S    | GND           | Signal Ground                                                |
| 178     | O    | LAN1_LINK1000 | Gigabit Ethernet Indicator Signal                            |
| 180     | O    | LAN1_LINK100  | Fast Ethernet Indicator Signal                               |
| 182     | O    | LAN1_LINKACT  | Network Port Status Indicator Signal                         |
| 184     | O    | EDP_VDD_EN    | Core Board EDP Display VDD Power Enable Control              |
| 186     | O    | EDP_BKLT_CTRL | Core Board EDP Display Backlight Adjustment Signal           |
| 188     | O    | EDP_BKLEN     | Core Board EDP Display Backlight Power Enable Control        |
| 189     | S    | GND           | Signal Ground                                                |
| 191     | O    | LVDS_RST#     | LVDS Reset Signal                                            |
| 193     | O    | LVDS_LINK     | LVDS Connection Status Signal                                |
| 195     | I    | LVDS_6B_8B#   | LVDS Data Encoding Configuration Signal                      |
| 197     | S    | GND           | Signal Ground                                                |
| 199     | O    | EDP_TXN1      | Core Board EDP Display lane 1 Negative Signal (EDP_D1_N)     |
| 201     | O    | EDP_TXP1      | Core Board EDP Display lane 1 Positive Signal (EDP_D1_P)     |
| 203     | S    | GND           | Signal Ground                                                |
| 205     | O    | EDP_TXN0      | Core Board EDP Display lane 0 Negative Signal (EDP_D0_N)     |
| 207     | O    | EDP_TXP0      | Core Board EDP Display lane 0 Positive Signal (EDP_D0_P)     |

| MXM NO. | Type | Function   | Remark                                                        |
|---------|------|------------|---------------------------------------------------------------|
| 209     | S    | GND        | Signal Ground                                                 |
| 211     | I    | SATA1_RXN  | Core Board SATA lane 1 Receive Negative Signal (SATA_RX1_N)   |
| 213     | I    | SATA1_RXP  | Core Board SATA lane 1 Receive Positive Signal (SATA_RX1_P)   |
| 215     | S    | GND        | Signal Ground                                                 |
| 217     | I    | SATA0_RXN  | Core Board SATA lane 0 Receive Negative Signal (SATA_RX0_N)   |
| 219     | I    | SATA0_RXP  | Core Board SATA lane 0 Receive Positive Signal (SATA_RX0_P)   |
| 221     | S    | GND        | Signal Ground                                                 |
| 223     | O    | COME_TXD   | Core Board Serial Port E Transmit Data (UART_E_TXD)           |
| 225     | I    | COME_RXD   | Core Board Serial Port E Receive Data (UART_E_RXD)            |
| 227     | O    | COMD_TXD   | Core Board Serial Port D Transmit Data (UART_D_TXD)           |
| 229     | I    | COMD_RXD   | Core Board Serial Port D Receive Data (UART_D_RXD)            |
| 231     | O    | COMC_TXD   | Core Board Serial Port C Transmit Data (UART_C_TXD)           |
| 233     | I    | COMC_RXD   | Core Board Serial Port C Receive Data (UART_C_RXD)            |
| 235     | I    | COMA_DCD#  | Core Board Serial Port A Data Carrier Detect (UART_A_DCD)     |
| 237     | I    | COMA_RI#   | Core Board Serial Port A Ring Indicator (UART_A_RI)           |
| 239     | I    | COMA_CTS#  | Core Board Serial Port A Clear To Send (UART_A_CTS)           |
| 241     | O    | COMA_DTR#  | Core Board Serial Port A Data Terminal Ready (UART_A_DTR)     |
| 243     | O    | COMA_RTS#  | Core Board Serial Port A Request To Send (UART_A_RTS)         |
| 245     | I    | COMA_DSR#  | Core Board Serial Port A Data Set Ready (UART_A_DSR)          |
| 247     | O    | COMA_TXD   | Core Board Serial Port A Transmit Data (UART_A_TXD)           |
| 249     | I    | COMA_SIN   | Core Board Serial Port A Receive Data (UART_A_RXD)            |
| 251     | S    | GND        | Signal Ground                                                 |
| 253     | O    | DDI1_TXN0  | Core Board DDI1 Display lane 0 Negative Signal (DDI1_D0_N)    |
| 255     | O    | DDI1_TXP0  | Core Board DDI1 Display lane 0 Positive Signal (DDI1_D0_P)    |
| 257     | S    | GND        | Signal Ground                                                 |
| 259     | O    | DDI1_TXN1  | Core Board DDI1 Display lane 1 Negative Signal (DDI1_D1_N)    |
| 261     | O    | DDI1_TXP1  | Core Board DDI1 Display lane 1 Positive Signal (DDI1_D1_P)    |
| 263     | S    | GND        | Signal Ground                                                 |
| 265     | O    | DDI1_TXN2  | Core Board DDI1 Display lane 2 Negative Signal (DDI1_D2_N)    |
| 267     | O    | DDI1_TXP2  | Core Board DDI1 Display lane 2 Positive Signal (DDI1_D2_P)    |
| 269     | S    | GND        | Signal Ground                                                 |
| 271     | O    | DDI1_TXN3  | Core Board DDI1 Display lane 3 Negative Signal (DDI1_D3_N)    |
| 273     | O    | DDI1_TXP3  | Core Board DDI1 Display lane 3 Positive Signal (DDI1_D3_P)    |
| 275     | S    | GND        | Signal Ground                                                 |
| 277     | IO   | DDI1_AUXN  | Core Board DDI1 Display AUX lane Negative Signal (DDI1_AUX_N) |
| 279     | IO   | DDI1_AUXP  | Core Board DDI1 Display AUX lane Positive Signal (DDI1_AUX_P) |
| 281     | I    | DDI1_HPD_C | Core Board DDI1 Display Hot Plug Detect Signal (DDI1_HPD)     |
| 190     | I    | EDP0_HPD   | Core Board EDP Display Hot Plug Detect Signal (EDP_HPD)       |
| 192     | IO   | EDP_AUX_DN | Core Board EDP Display AUX lane Negative Signal (EDP_AUX_N)   |
| 194     | IO   | EDP_AUX_DP | Core Board EDP Display AUX lane Positive Signal (EDP_AUX_P)   |
| 196     | S    | GND        | Signal Ground                                                 |
| 198     | O    | EDP_TXN3   | Core Board EDP Display lane 3 Negative Signal (EDP_D3_N)      |

| MXM NO. | Type | Function     | Remark                                                       |
|---------|------|--------------|--------------------------------------------------------------|
| 200     | O    | EDP_TXP3     | Core Board EDP Display lane 3 Positive Signal (EDP_D3_P)     |
| 202     | S    | GND          | Signal Ground                                                |
| 204     | O    | EDP_TXN2     | Core Board EDP Display lane 2 Negative Signal (EDP_D2_N)     |
| 206     | O    | EDP_TXP2     | Core Board EDP Display lane 2 Positive Signal (EDP_D2_P)     |
| 208     | S    | GND          | Signal Ground                                                |
| 210     | O    | SATA1_TXN    | Core Board SATA lane 1 Transmit Negative Signal (SATA_TX1_N) |
| 212     | O    | SATA1_TXP    | Core Board SATA lane 1 Transmit Positive Signal (SATA_TX1_P) |
| 214     | S    | GND          | Signal Ground                                                |
| 216     | O    | SATA0_TXN    | Core Board SATA lane 0 Transmit Negative Signal (SATA_TX0_N) |
| 218     | O    | SATA0_TXP    | Core Board SATA lane 0 Transmit Positive Signal (SATA_TX0_P) |
| 220     | S    | GND          | Signal Ground                                                |
| 222     | O    | COMF_TXD     | Core Board Serial Port F Transmit Data (UART_F_TXD)          |
| 224     | I    | COMF_RXD     | Core Board Serial Port F Receive Data (UART_F_RXD)           |
| 226     | I    | COMB_DCD#    | Core Board Serial Port B Data Carrier Detect (UART_B_DCD)    |
| 228     | I    | COMB_RI#     | Core Board Serial Port B Ring Indicator (UART_B_RI)          |
| 230     | I    | COMB_CTS#    | Core Board Serial Port B Clear To Send (UART_B_CTS)          |
| 232     | O    | COMB_DTR#    | Core Board Serial Port B Data Terminal Ready (UART_B_DTR)    |
| 234     | O    | COMB_RTS#    | Core Board Serial Port B Request To Send (UART_B_RTS)        |
| 236     | I    | COMB_DSR#    | Core Board Serial Port B Data Set Ready (UART_B_DSR)         |
| 238     | O    | COMB_TXD     | Core Board Serial Port B Transmit Data (UART_B_TXD)          |
| 240     | I    | COMB_RXD     | Core Board Serial Port B Receive Data (UART_B_RXD)           |
| 242     | S    | GND          | Signal Ground                                                |
| 244     | O    | DDI2_TXN1    | Core Board DDI2 Display lane 1 Negative Signal (DDI2_D1_N)   |
| 246     | O    | DDI2_TXP1    | Core Board DDI2 Display lane 1 Positive Signal (DDI2_D1_P)   |
| 248     | S    | GND          | Signal Ground                                                |
| 250     | O    | DDI2_TXN2    | Core Board DDI2 Display lane 2 Negative Signal (DDI2_D2_N)   |
| 252     | O    | DDI2_TXP2    | Core Board DDI2 Display lane 2 Positive Signal (DDI2_D2_P)   |
| 254     | S    | GND          | Signal Ground                                                |
| 256     | O    | DDI2_TXN3    | Core Board DDI2 Display lane 3 Negative Signal (DDI2_D3_N)   |
| 258     | O    | DDI2_TXP3    | Core Board DDI2 Display lane 3 Positive Signal (DDI2_D3_P)   |
| 260     | S    | GND          | Signal Ground                                                |
| 262     | O    | DDI2_TXN0    | Core Board DDI2 Display lane 0 Negative Signal (DDI2_D0_N)   |
| 264     | O    | DDI2_TXP0    | Core Board DDI2 Display lane 0 Positive Signal (DDI2_D0_P)   |
| 266     | S    | GND          | Signal Ground                                                |
| 268     | IO   | DDI2_AUXN    | Core board DDI2 Display lane AUX Negative signal             |
| 270     | IO   | DDI2_AUXP    | Core board DDI2 Display lane AUX Positive signal             |
| 272     | I    | DDI2_HPD_C   | Core board DDI2 Display lane HPD signal                      |
| 274     | IO   | DDI2_DDC_SCL | Core board DDI2 Display lane DDC CLK signal                  |
| 276     | IO   | DDI2_DDC_SDA | Core board DDI2 Display lane DDC DATA signal                 |
| 278     | IO   | DDI1_DDC_SCL | Core board DDI1 Display lane DDC CLK signal                  |
| 280     | IO   | DDI1_DDC_SDA | Core board DDI1 Display lane DDC DATA signal                 |
|         |      |              |                                                              |

## Chapter 3 Installation Instructions

### 3.1 Cooler Installation Instructions

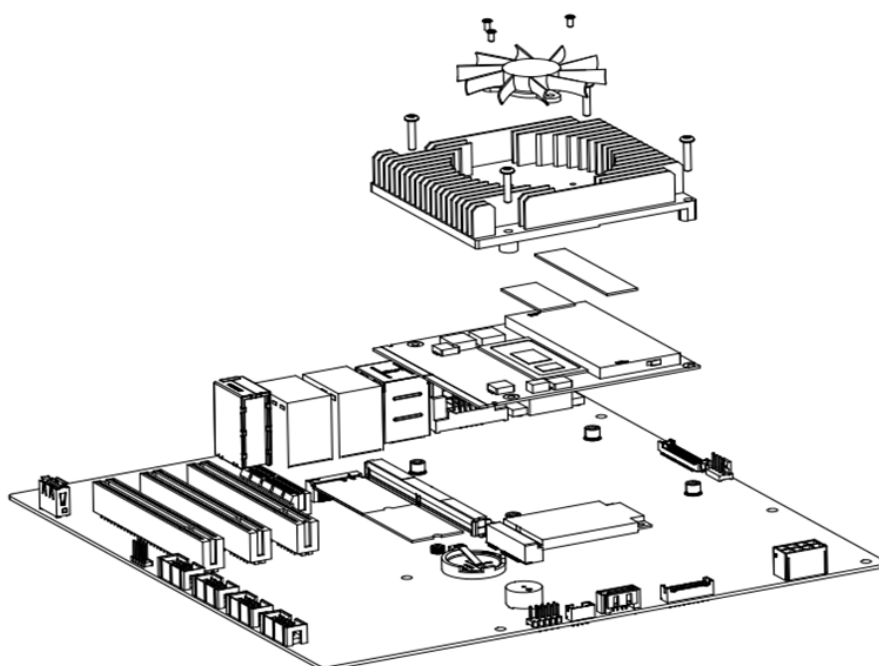
Step 1. Insert the core board into the carrier board interface, and install the motherboard standoffs. Screw the six M3 standoffs into the corresponding threaded holes on the motherboard.

Step 2. Apply thermal pads onto the CPU, bridge chip, and memory modules. Install the cooler by aligning its six M3×10L screws with the standoff holes on the motherboard, then fasten the screws.

Step 3. Secure the fan to the cooler using four M3×18 screws, fastening them into the fan mounting holes.

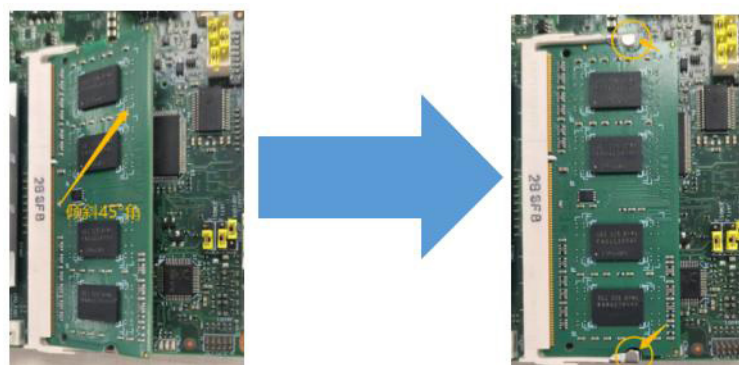
Step 4. Connect the cooler fan power cable to the FAN header on the carrier board (Caution: Fan operates at 12V).

Detailed operations are shown in the figure below:



### 3.2 SO-DIMM Memory Installation Instructions

Hold the SO-DIMM module at a 45-degree angle and insert it into the memory slot. Press down firmly until the retention clips on both sides engage automatically.



## Chapter 4 AMI BIOS Settings

The AMI BIOS ROM has a built-in setup program that stores the computer's most important basic input/output programs, allowing users to modify basic system configurations. After setting, the system configuration is saved in the motherboard's FLASH. When the power is off, the onboard battery provides the necessary power to the FLASH to retain the settings. When the power is on, press the <Del> or <Esc> key during the POST process to access the CMOS SETUP screen. The interface is divided into left and right columns. The left column displays gray for non-configurable options and blue for configurable options. The right column displays a description of the selected option in the left column and shortcut key operations at the bottom.

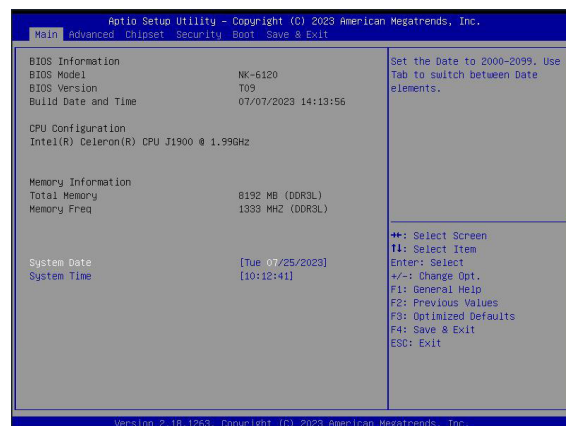
### 4.1 Shortcut Key Instructions

| Hot Key            | Function                          | Description           |
|--------------------|-----------------------------------|-----------------------|
| < ← > >            | BIOS interface selection          | Within BIOS interface |
| < ↑ > > ↓ >        | BIOS option selection             | Within BIOS interface |
| <CTRL>+<ALT>+<DEL> | Restart system                    | After system power-on |
| <Enter>            | Confirm selection                 | Within BIOS interface |
| <DEL>              | Enter BIOS setup interface        | Within BIOS interface |
| <ESC>              | Exit BIOS setup interface         | After system power-on |
| <F3>               | Load default                      | Within BIOS interface |
| <F4>               | Save settings and exit            | Within BIOS interface |
| <F7>               | Call BIOS quick start option menu | After system power-on |

### 4.2 Main Interface

After the system starts, press <Del> to enter the BIOS setup interface. The main menu will appear on the screen. Use the arrow keys to navigate through the options and press <Enter> to enter the submenu.

The Main interface is the first interface users see when entering the BIOS. It allows users to check BIOS version, CPU, memory, and other related information, as well as set the system date and time. The Main interface is shown below:

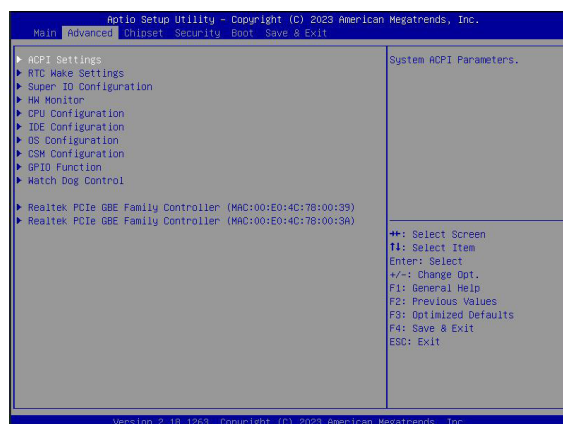


#### 4.2.1 System Date and Time Settings

Select System Date or System Time to change the system date and time. Use the <Tab> key or < ← > > to move between fields. The system date format is "Month/Day/Year," and the system time is in 24-hour format as "Hour:Minute:Second ." Use the "+, " -, " and number keys to modify the values. Press Enter to switch between Month/Day/Year or Hour/Minute/Second. After setting, press F4 to save the settings, which will take effect after a restart.

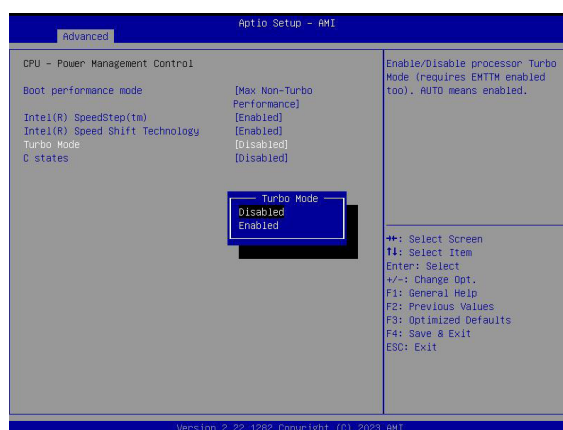
### 4.3 Advanced Interface

Enter the Advanced interface to configure system functions. It provides access to advanced system settings, including CPU settings, memory settings, SATA settings, overclocking settings, virtualization options, and more. Use the <↑> <↓> keys to select and <Enter> to enter the settings. This section introduces the Advanced settings.



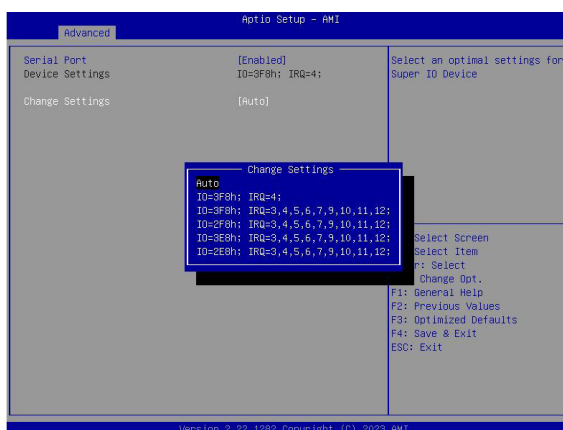
#### 4.3.1 Turbo Mode Settings

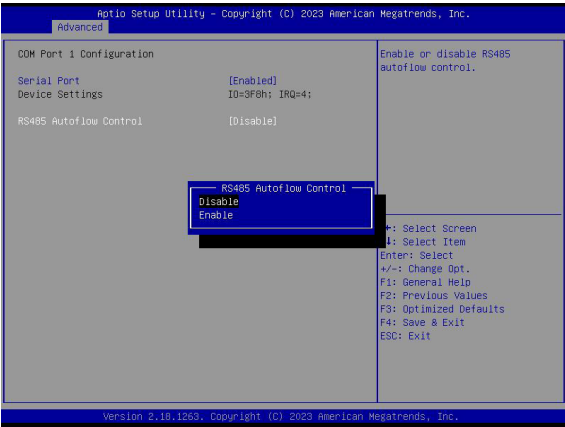
In the Advanced interface, navigate to Power & Performance -> CPU - Power Management Control -> Turbo Mode to enable or disable overclocking mode. The default is Disabled.



#### 4.3.2 TPM Function Settings

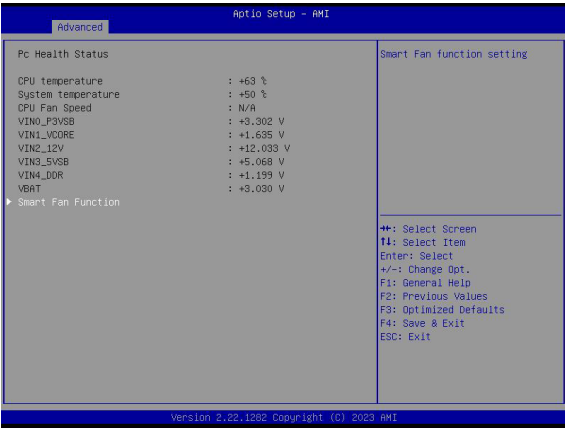
In the Advanced interface, navigate to Trusted Computing -> Security Device Support to enable or disable TPM functionality. After setting, press F4 to save and exit. The system will restart to apply the changes.



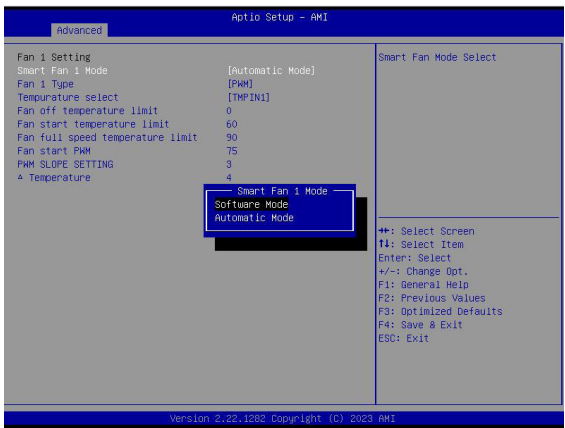


4.3.3 HW Monitor & Smart Fan

In the Advanced interface, select Hardware Monitor to display CPU temperature, system temperature, key voltage parameters, and Smart Fan Function information.

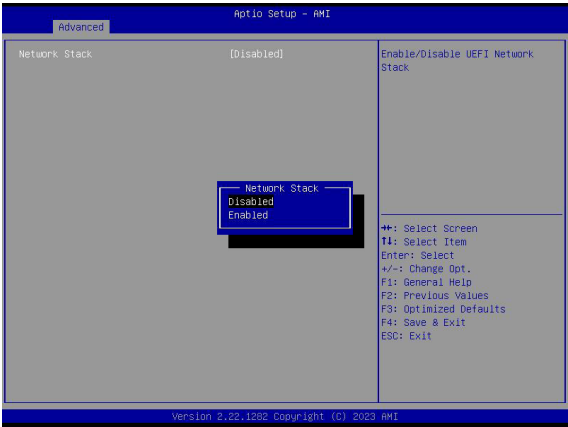


Smart Fan Function: You can set the Smart Fan Mode to Software mode or Automatic mode (default). In Software mode, you can set the system temperature risk value, fan start temperature, fan stop temperature, fan mode, duty cycle, etc., based on user application requirements.



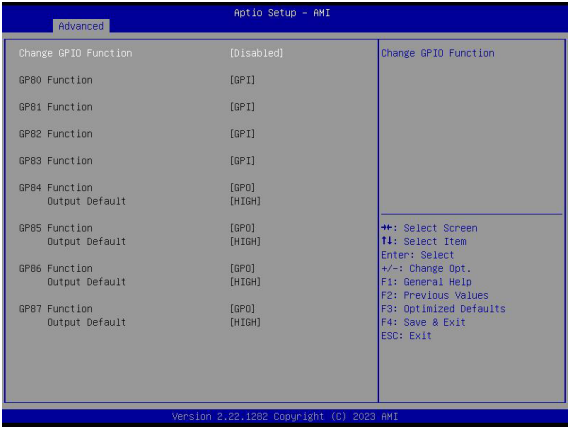
4.3.4 Wake-on-LAN

In the Advanced interface, navigate to Network Stack Configuration -> Network Stack to enable or disable Wake-on-LAN functionality. The default is Disabled. After setting, press F4 to save and exit. The system will restart to apply the changes.



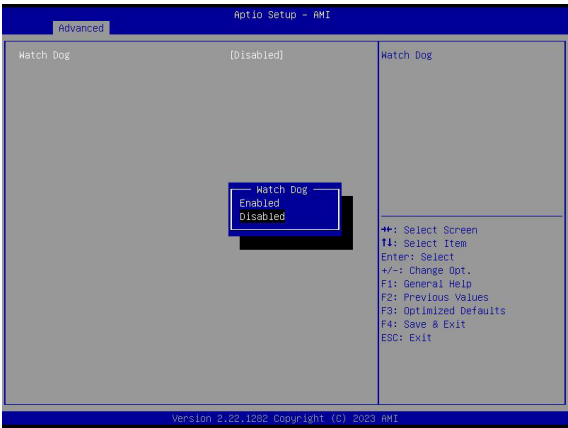
4.3.5 GPIO Settings

In the Advanced interface, go to Network Stack Configuration → Network Stack to enable or disable the Wake-on-LAN function. The default setting is Disabled. After configuration, press F4 to save and exit. A system restart is required for the changes to take effect.



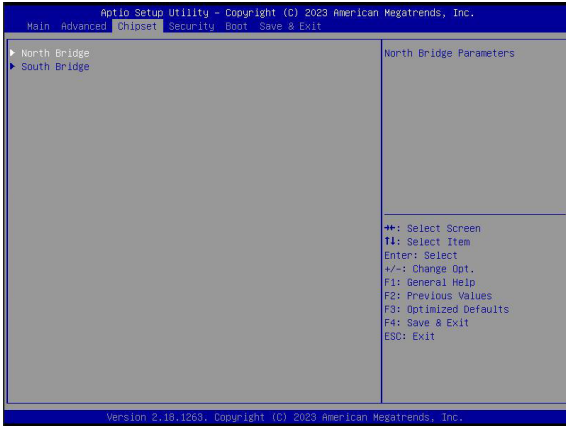
4.3.6 Watch Dog Settings

In the Advanced interface, navigate to Watch Dog Control -> Watch Dog to enable or disable the Watchdog function. The default is Disabled. After setting, press F4 to save and exit. For detailed usage, refer to Appendix 3.



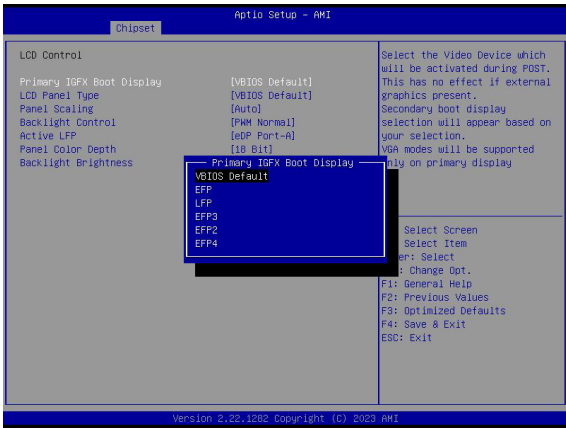
4.4 Chipset Interface

Enter the Chipset interface to configure the computer's chipset options. The chipset is the integrated circuit that connects the components on the motherboard. The settings here may involve PCIe configuration, USB configuration, hard drive controller settings, etc. Use the < ↑ > < ↓ > keys to select and <Enter> to enter the settings. This section introduces the Chipset settings.



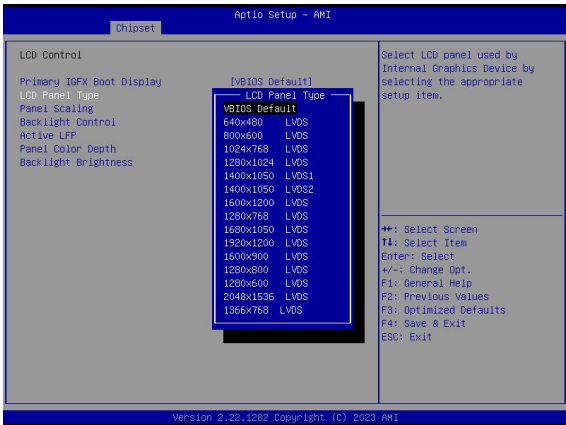
4.4.1 Display Priority

In the Chipset interface, navigate to System Agent (SA) Configuration -> Graphics Configuration -> LCD Control -> Primary IGFX Boot Display to set the display priority for the integrated graphics card in the system (EFP(DVI-D)/LFP(LVDS)/EFP3(DP2)/EFP2(DP1)/EFP4(DP3)). After setting, press F4 to save and exit. The system will restart to apply the changes.



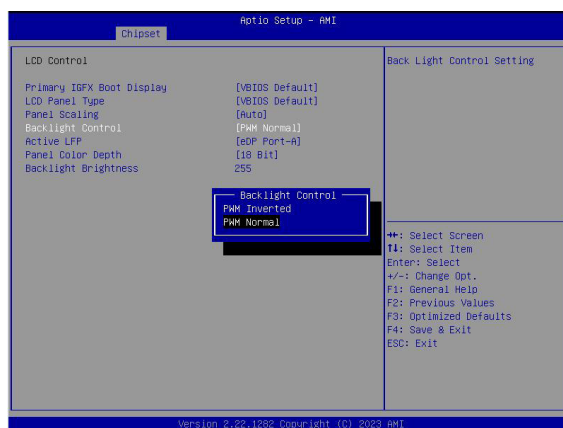
4.4.2 LVDS Resolution Settings

In the Chipset interface, navigate to System Agent (SA) Configuration -> Graphics Configuration -> LCD Control -> LCD Panel Type to set the LVDS resolution. After setting, press F4 to save and exit. The system will restart to apply the changes.



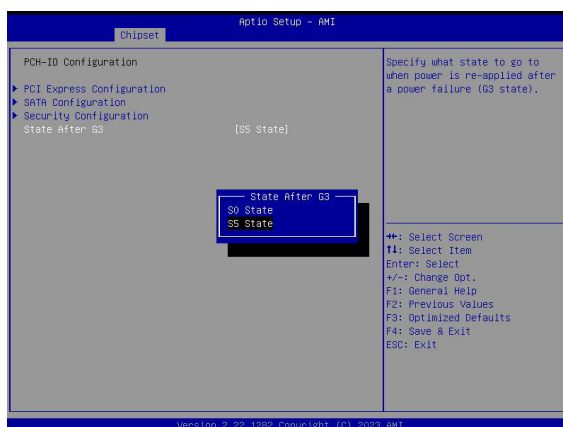
### 4.4.3 Backlight Brightness Inversion Mode

In the Chipset interface, navigate to System Agent (SA) Configuration -> Graphics Configuration -> LCD Control -> LCD Panel Minimum Brightness to set the LCD screen's minimum brightness to normal (PWM Normal) or inverted (PWM Inverted) mode. After setting, press F4 to save and exit. The system will restart to apply the changes.



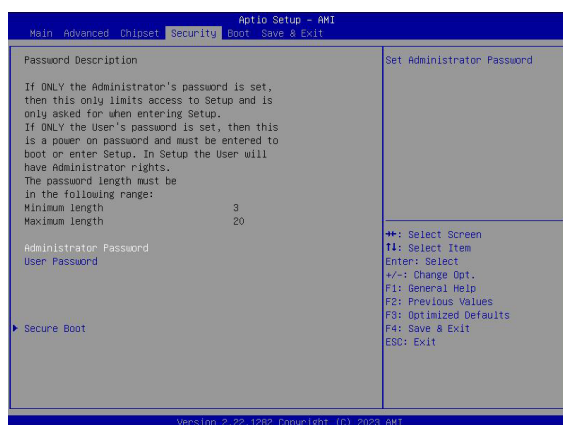
### 4.4.4 Power-on Auto Start

In the Chipset interface, navigate to PCH-IO Configuration -> State after G3 to enable or disable power-on auto start. Power on is AT mode, where the system powers on automatically when power is connected. Power off is ATX mode, where the system requires pressing the power button to start. The default is Power off. After setting, press F4 to save and exit. The system will restart to apply the changes.



### 4.5 Security Interface

Enter the Security interface to set password protection and other security functions. Select to enter the settings for administrator and user password protection options to enter the submenu. Use the <↑> <↓> keys to select and <Enter> to enter the settings. This section introduces the Security settings.



4.5.1 Administrator Password Settings

In the Security interface, select Administrator Password, press Enter, and use the keyboard to enter a password of six or more characters, including letters, numbers, and symbols. After setting, press F4 to save the settings. The system will restart to apply the changes.

4.5.2 User Password Settings

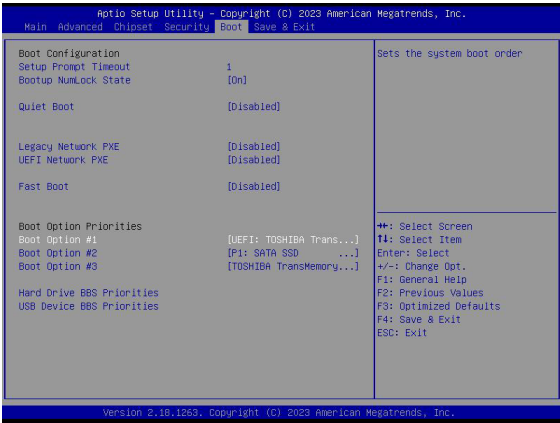
In the Security interface, select User Password, press Enter, and use the keyboard to enter a password of six or more characters, including letters, numbers, and symbols. After setting, press F4 to save the settings. The system will restart to apply the changes.



**After setting the password, please remember it. Otherwise, you will not be able to access the system without the password, resulting in additional repair costs.**

4.6 BOOT Interface

Enter the BOOT interface to set the system boot order, select boot options, and set the boot interface. Use the < ↑ > < ↓ > keys to select and <Enter> to enter the settings. This section introduces the BOOT settings.



4.6.1 Set Num Lock State at Boot

In the BOOT interface, select Boot Num Lock State to enable or disable the Num Lock key on the keyboard at boot. After setting, press F4 to save the settings. The system will restart to apply the changes.

4.6.2 Set Boot Logo

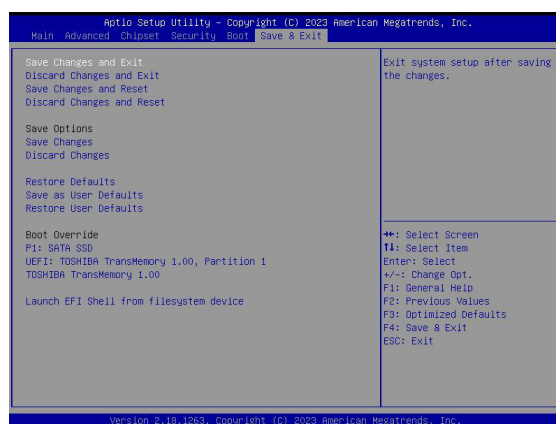
In the BOOT interface, select Quiet Boot to enable or disable the boot logo. Select "Enable" to show the boot logo, or "Disable" to hide it. After setting, press F4 to save the settings. The system will restart to apply the changes.

4.6.3 Set Boot Order

In the BOOT interface, select Boot Option Priorities to set the boot device order. Boot Option #1 is the first boot device, Boot Option #2 is the second, and so on. After setting, press F4 to save the settings. The system will restart to apply the changes.

## 4.7 Save & Exit Interface

Enter the Save & Exit interface to load or save settings and exit the BIOS parameter settings. Select to save and exit the BIOS parameter settings to enter the submenu. Use the < ↑ > < ↓ > keys to select and <Enter> to enter the settings. This section introduces the Save & Exit settings.



### 4.7.1 Save Changes and Reset

In the Save & Exit interface, select Save Changes and Reset, press F4 to save the settings, and the system will restart to apply the changes.

### 4.7.2 Discard Changes and Reset

In the Save & Exit interface, select Discard Changes and Reset, press F4 to save the settings, and the system will restart without applying the changes.

### 4.7.3 Restore Default Settings

In the Save & Exit interface, select Restore Defaults, press F4 to save the settings, and the system will restart to apply the default settings.

### 4.7.4 Set Boot Device Priority

In the Save & Exit interface, select Boot Override, press F4 to save the settings, and the system will restart to apply the changes.

Appendix 1 Watchdog Example

```
IoWrite8(0x2E,0x88);
    IoWrite8(0x2E,0x88); //SIO ENTER
    IoWrite8(0x2E, 0x07); //watchdog
    IoWrite8(0x2F, 0x08);

    if(gWatchdogmode==0)
    {
        IoWrite8(0x2E, 0xF1);
        IoWrite8(0x2F, 0x00); //disable watch dog
    }
    else if(gWatchdogmode==1)
    {
        IoWrite8(0x2E, 0xF0);
        IoWrite8(0x2F, 0x00);
        IoWrite8(0x2E, 0xF1);
        IoWrite8(0x2F, gWatchdogvalue); //SEC MODE
    }
    else
    {
        IoWrite8(0x2E, 0xF0);
        IoWrite8(0x2F, 0x08);
        IoWrite8(0x2E, 0xF1);
        IoWrite8(0x2F, gWatchdogvalue); //MIN MODE
    }

    IoWrite8(0x2E, 0xAA); //EXIT SIO
```